METHOD AND STRUCTURE FOR A WAFER LEVEL PACKAGING

A method and structure for a wafer level package is provided, which utilizes a plurality of spacer walls on a semiconductor wafer or a transparent substrate, which has the ability to decide the position of the sealant. As a result, the dimension of a device is decided by the position of the sealant and the spacer walls, therefore, shrinking the distance between the photosensitive zone and the sealant will enhance the gross dies after performing a die sawing process to the whole semiconductor wafer. In addition, the semiconductor process decides the height of the spacer walls so that the yield will be improved due to the fact that a uniformity of the gap, which is between the semiconductor wafer and the transparent substrate, and the width of sealant, will be controlled.